EENG 5550 HW 1

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# Block diagram of 4 bit computational unit

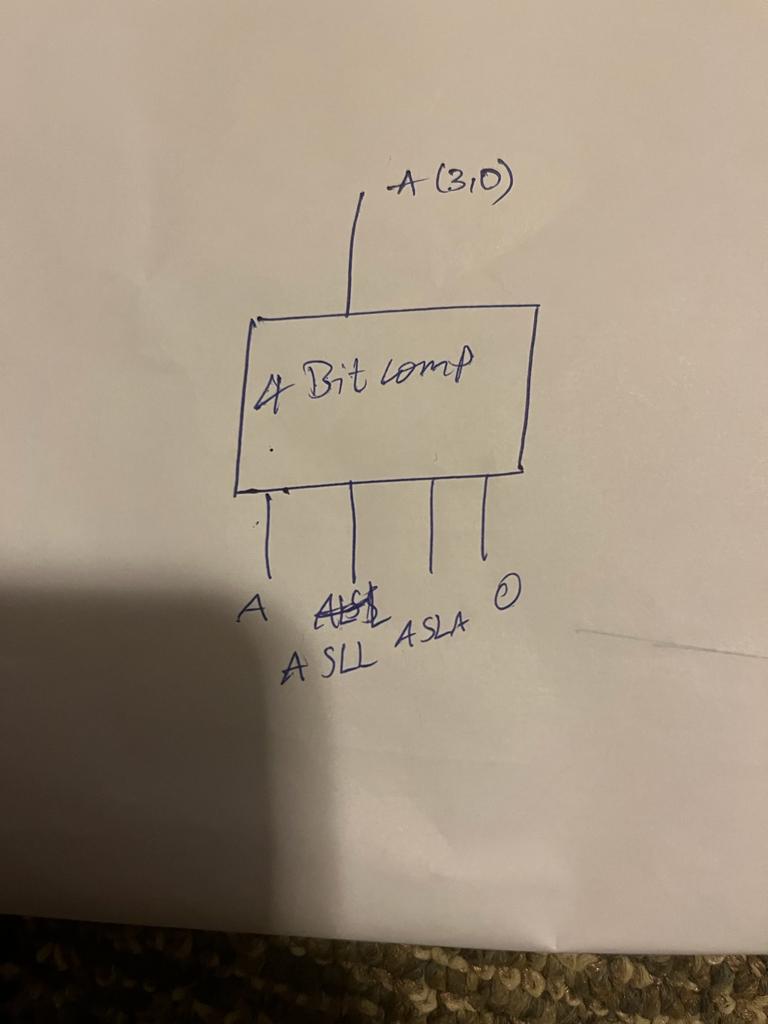


Figure 4 bit computational unit

* Overall Component: 4 bit computational unit
* Overall ports:
  + Inputs: A
    - Sel
  + Outputs:
    - Y
* Necessary intermediate signals:
  + A
  + Sel
  + Y

## Design\Algorithm ex:

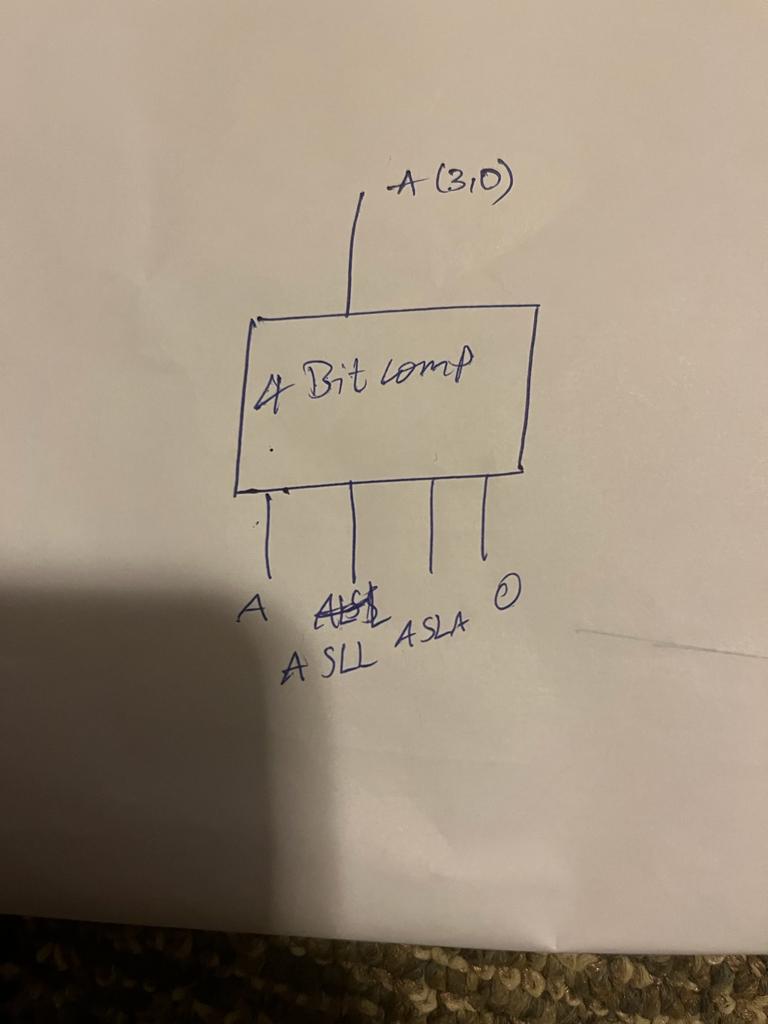


Figure 2– 4 bit computational unit

* Overall Component: 32:1 multiplexer (mux)
* Overall ports:
  + Inputs:
    - A: 4 bits -> 1001
    - A: 4 bits -> 0001
    - A: 4 bits -> 0011
    - A: 4 bits -> 0101
    - Sel: 2bits -> select line input
      * Sel: 00
      * Sel: 01
      * Sel: 10
      * Sel: 11
  + Outputs:
    - :Y single bit -> output

**Representation of design:**

|  |  |
| --- | --- |
| Select input | Resulting output |
| 00 | A |
| 01 | A shift left |
| 10 | A shift right |
| 11 | 0 |

# Generated RTL Block Diagram\Schematic

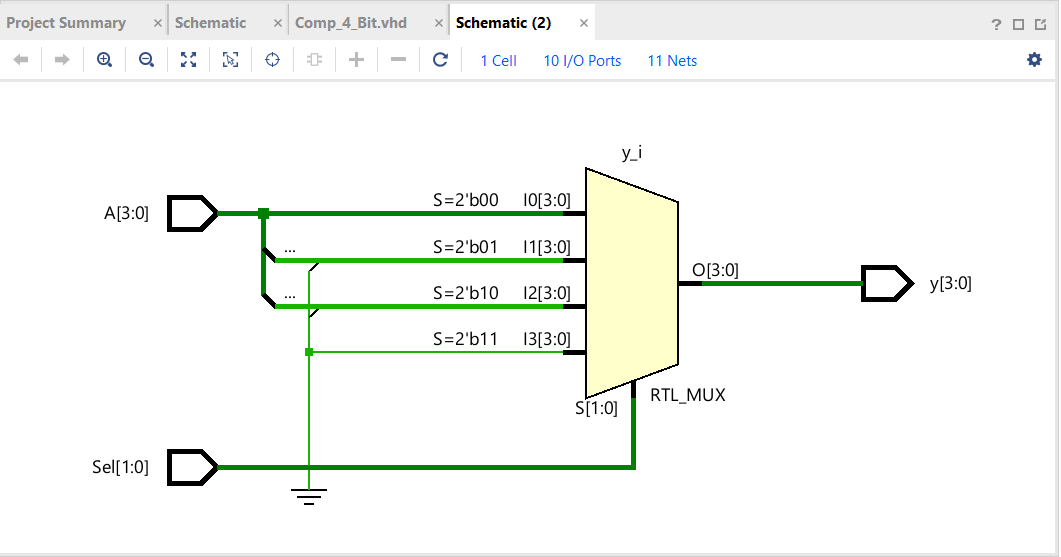


Figure 5 - generated RTL schematic.

# Results

## Waveforms

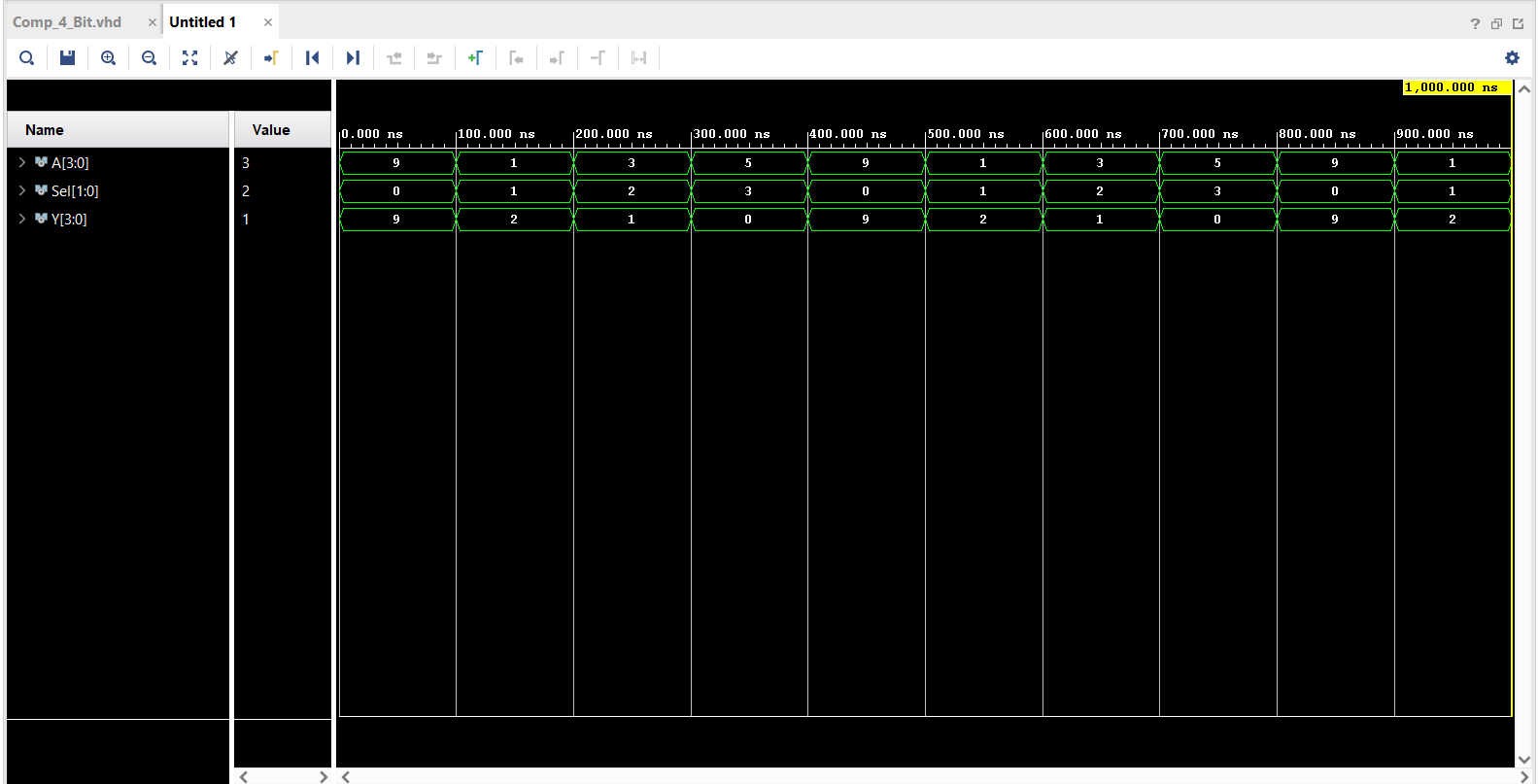


Figure 6 - Waveforms

## Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | calculations | waveforms |  |
|  | Sel | Y | Y | |
| Test case 1: | 10000 | 10010 | 10010 | |
| Test case 2: | 10010 | 10010 | 10010 | |